AMENDMENTS TO THE CLAIMS

1. (currently amended) A system for implementing arbitration between one or more shared peripheral core devices in a system on chip (SOC) integrated circuit architecture, comprising:

a first microprocessor in communication with a first system bus;

a second microprocessor in communication with a second system bus;

at least one peripheral core device accessible by both said first microprocessor and said second microprocessor; and

an arbitration unit in communication with said first system bus and said second system bus,;

~~wherein~~ said arbitration unit ~~is~~ configured to control communication between said at least one peripheral core device and said first and second microprocessors;

said arbitration unit further comprising:

a first buffer device coupled to said first system bus, a second buffer device coupled to said second system bus, input multiplexing circuitry in communication with said first buffer device, said second buffer device and said at least one peripheral core device, and arbitration logic in communication with said first buffer device, said second buffer device and said input multiplexing circuitry;

external multiplexing circuitry in communication with said at least one peripheral core device and said external connections; and

an external buffer device coupled between said external multiplexing circuitry and said external connections;

said arbitration logic configured to:

detect a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors;

determine the existence of a free peripheral from said at least one

peripheral core device; and

implement communication between a determined free peripheral and said requesting one of said first and second microprocessors, and inform said requesting one of said first and second microprocessors whenever no free peripheral is presently available;

said at least one peripheral core device further configured to communicate, at any time, data to and from the SOC integrated circuit architecture through an associated external connection for each of said first and second microprocessors.

2. (original) The system of claim 1, further comprising a plurality of arbitration units, wherein each of said plurality of arbitration units is configured to control communication between said first system bus and said second system bus, and a group of peripheral core devices associated therewith.

3-9. (cancelled)

10. (currently amended) The system of claim 91, wherein:

said arbitration unit is configured to arbitrarily receive incoming data from one of said external connections and identify a target destination for said incoming data;

said arbitration unit is configured to internally note an assignment between a free peripheral and said target destination; and

said arbitration unit is configured to maintain said assignment until the completion of a completed data transfer between said one of said external connections and said target destination, through said free peripheral.

11. (currently amended) A method for implementing arbitration between one or more shared peripheral core devices in a system on chip (SOC) integrated circuit architecture, the method comprising:

configuring a first microprocessor in communication with a first system bus;

configuring a second microprocessor in communication with a second system bus;

configuring at least one peripheral core device to be accessible by both said first microprocessor and said second microprocessor; and

configuring an arbitration unit in communication with said first system bus and said second system bus, wherein said arbitration unit controls communication between said at least one peripheral core device and said first and second microprocessors;

said arbitration unit further comprising:

a first buffer device coupled to said first system bus, a second buffer device coupled to said second system bus, input multiplexing circuitry in communication with said first buffer device, said second buffer device and said at least one peripheral core device, and arbitration logic in communication with said first buffer device, said second buffer device and said input multiplexing circuitry;

external multiplexing circuitry in communication with said at least one peripheral core device and said external connections; and

an external buffer device coupled between said external multiplexing circuitry and said external connections;

said arbitration logic configured to:

detect a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors;

determine the existence of a free peripheral from said at least one peripheral core device; and

implement communication between a determined free peripheral

and said requesting one of said first and second microprocessors, and inform said requesting one of said first and second microprocessors whenever no free peripheral is presently available;

said at least one peripheral core device further configured to communicate, at any time, data to and from the SOC integrated circuit architecture through an associated external connection for each of said first and second microprocessors.

12. (original) The method of claim 11, further comprising a configuring plurality of arbitration units to control communication between said first system bus and said second system bus, and a group of peripheral core devices associated therewith.

13-19. (cancelled)

20. (currently amended) The method of claim ~~19~~11, wherein:

said arbitration unit arbitrarily receives incoming data from one of said external connections and identifies a target destination for said incoming data;

said arbitration unit internally notes an assignment between a free peripheral and said target destination; and

said arbitration unit maintains said assignment until the completion of a completed data transfer between said one of said external connections and said target destination, through said free peripheral.